STAR scaler board

May 3, 2002

PROM version: H

Address (HEX)	read/write	Register name
0	r	Board ID (HEX: deadf0c0)
4	rw	scaler active
8	rw	Memory bank Bit(0): (0=A, 1=B); Bit(1)=1: A+B (reading)
10	rw	event counter LSB
14	rw	event counter MSB
20	w	Bit(0)=1 initiates a automated memory clear
24	r	Bit(0)=1 indicated board is busy clearing the memory
30	w	Bit(0)=1 starts the zero suppression Bit(1)=1 resumes the zero suppression
34	r	Bit(0)=1 indicates zero suppression done (no more non zero events)
38	r	Bit(0)=1 indicates board is busy doing zero suppression
3c	r	number of events in the "zero suppression buffer"
100-15c	rw	Delay register (100-input 0; 15c-input 23)
200-25c	rw	Vernier delay register (200-input 0; 25c-input 23)
300-35c	r	positive phase offset meter (300-input 0; 35c-input 23)
400-45c	r	negative phase offset meter (400-input 0; 45c-input 23)
10000-11ffc	r	zero suppression buffer

Table 1: Register addresses

There are two sets of delay registers. The "Delay registers" and the "Vernier delay registers". The "Delay registers" are 4 bits wide and delays delay the input bit by increments of one RHIC. The "Vernier delay registers" are 3 bits wide and delay the input bits by increments of $12.5ns$.

The "Phase offset meter" gives the time from the negative edge of RHIC to a positive/negative edge of the input bit. The time is given in internal

board clock cycles ($12.5ns$). This value gets updated every time there is a change of the input signal.

Bit	Function
0	active master (gated with RUN_STOP_N)
1	active slave (gated with RUN_STOP_N)
2	force active master
3	force active slave

Table 2: scaler active register

The zero suppression feature copies the channels with a non zero histogram value to the "zero suppression buffer". There are 4 register to control this. The "start" bit starts the zero suppression at channel 0. The "resume" bit allows to continue a zero suppression in the case there are more non zero channels than there is space in the "zero suppression buffer". The "busy" bit indicates the board is busy to do the zero suppression. The busy time depends on the amount of non zero channels and their location in the histogram memory. The maximum time is about 3 to 4 seconds. The "done" bit indicates there are no more non zero channels in the histogram memory. The register "3c" shows how much information is in the "zero suppression buffer" in case there are less non zero channels than there is space in the "zero suppression buffer".

Address (hex)	Function	
X0010000	LSB of counter	
X0010004	channel number(24 bit in MSB)	MSB of counter
⋮	⋮	

Table 3: zero suppression buffer memory map

The histogram is at the "board base address + 0x8000000 + channel * 8". In order to read or write the memory, the board has to be inactive.
"board base address + 0x8000000 + channel * 8" contains the lower 32 bit.
"board base address + 0x8000000 + channel * 8 + 4" contains the upper 8 bit.

Address (hex)	Function
X8000000	Channel 0 low 32 bit
X8000004	Channel 0 upper 8 bit
X8000008	Channel 1 low 32 bit
X800000c	Channel 1 upper 8 bit
⋮	⋮

Table 4: Data memory map

LED (from the top)	Function
1	Board active (histograming mode)
2	Memory selected in memory bank register (off: memory A; on: memory B)
3	VME access
4	not defined yet (blinking, board alive)

Table 5: Front panel LEDs

LEMO (from the top)	Function
1 (J5)	interconnection master slave
2 (J7)	"RUN_STOP_N" input on master

Table 6: LEMO connectors

Jumper	Function
S1 A28-A31	Board base address
S1 A24	Master (jumper)/Slave(no jumper)
J4	inter board communication (master: OUT; slave: IN)
J6	"RUN_STOP_N" (master: IN; slave: no jumper)

Table 7: Jumper